AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions of the claims and all prior listings of the claims in the present application.

1. (currently amended) A vestigial side band (VSB) synchronization (sync) signal detection circuit, comprising:

a data selector selecting one of a first data signal and a second data signal for output;

a pseudo-random number 511 (PN511) sequence detector receiving the selected first or second data signal, generating a plurality of correlation values for symbols of the received first or second data signal, outputting only those correlation values that exceed a first threshold as correlation values corresponding to a detected ~~Pseudo-random Number (PN)~~ PN511 sequence of a VSB signal, and outputting a first control signal related to sync signal generation;

a comparison buffer unit receiving the correlation values exceeding the first threshold from the PN511 sequence detector, storing a maximum correlation value among the received correlation values, generating a second control signal containing information regarding the position of a symbol in which the maximum correlation value is generated, comparing a next maximum correlation value to a second threshold, and generating a third control signal based on the result of comparison;

a sync signal position determination unit receiving the second control signal, determining positions of a next field sync signal and one or more segment sync signals, and generating a fourth control signal containing information regarding the positions of the next field sync signal and one or more segment sync signals based on the received second control signal;

a sync signal valid determination unit receiving the third and fourth control signals and generating at least one valid detection signal indicating that a generated field sync signal is valid based on a level of the third control signal and a level of the fourth control signal;

a finite state machine (FSM) that generates an internal lock signal in response to a valid detection signal, wherein the internal lock signal is fed back to the sync signal valid determination unit;

a pseudo-random number 63 (PN63) correlator receiving the selected first or second data signal from the data selector, detecting correlation values corresponding to a PN63 [[63]] sequence of the received first or second data signal, and generating a fifth control signal for determining the sign of [[the]] a field sync signal; and

a sync signal generator outputting one or more distinct types of sync signals in response to the first control signal, fourth control signal, fifth control signal, and [[the]] internal lock signal.

2. (currently amended) The circuit of claim 1, wherein the data selector selects the first data signal or the second data signal based on one or more of a level selection signal, an operation mode selection signal, a data selection signal, a lock selection signal, an external lock signal, and the internal lock signal.

3. (currently amended) The circuit of claim 1, wherein the PN511 sequence detector includes:

a sliding PN511 correlator that receives the symbols [[for]] of the selected first or second data signal and generates the correlation values for detecting the PN511 sequence; and

a correlation filter that receives the first threshold, selects correlation values larger than the first threshold for output as the correlation values corresponding to the PN511 sequence, and generates the first control signal for driving the sync signal generator to generate the plurality of distinct types of sync signals[[,]];

wherein the first threshold is provided for detection of [[a]] the field sync signal.

4. (currently amended) The circuit of claim 1, wherein the comparison buffer ~~circuit~~ unit compares the next maximum correlation value to the second threshold to determine whether the next maximum correlation value is a valid correlation value corresponding to the PN511 sequence.

5. (currently amended) The circuit of claim 1, wherein the comparison buffer unit includes:

a buffer for storing the maximum correlation value corresponding to the PN511 sequence, and for generating the second control signal; and

a comparator generating the third control signal at a first level, if the next maximum correlation value exceeds the second threshold, or else generating the third control signal at a second level.

6. (currently amended) The circuit of claim 5, wherein a value of the second threshold is set to a given percentage of the maximum correlation value[[s]] stored in the buffer.

7. (original) The circuit of claim 6, wherein the given percentage is 75%.

8. (currently amended) The circuit of claim 1, wherein the sync signal position determination unit includes:

a counting unit that counts [[the]] a number of the symbols so as to determine the positions of the next field sync and one or more segment sync signals, based on the symbol position information for the maximum correlation value contained in the second control signal; and

a calculator generating the fourth control signal at a first level, if positions of the next field sync and one or more segment sync signals are determined based on output from the counting unit, or else generating the fourth control signal at a second level.

9. (currently amended) The circuit of claim 8, wherein the counting unit further includes:

a first counter that counts 832 symbols to determine the position of [[the]] a next segment sync signal in response to the second control signal; and

a second counter that counts 313 segments to determine the position of the next field sync signal in response to the second control signal.

10. (currently amended) The circuit of claim 1, wherein the sync signal valid determination unit includes:

a valid detection signal generator that generates the at least one valid detection signal[[s]] at a first level if [[a]] the position of [[a]] the next field sync signal is validly detected based on each of the third and fourth control signals being at a first level; and

a lock detector that receives the internal lock signal from the FSM.

11. (currently amended) The circuit of claim 1, wherein the FSM includes:

a first shift register receiving valid detection signals;

a second shift register receiving the valid detection signals, each of the first and second shift registers storing the valid detection signals;

a level detector for detecting first levels and second levels of the valid detection signals stored in the first shift register, generating a first output signal at the first level if a number of the first-level valid detection signals is greater than [[the]] a number of the second-level valid detection signals, or else generating the first output signal at the second level;

a first OR gate that performs an OR operation on the valid detection signals stored in the second shift register and outputs the second output signal as the result of the OR operation;

a second OR gate that performs an OR operation on the internal lock signal and the first output signal;

an AND gate that performs an AND operation on an output of the second OR gate and the second output signal; and

a delayer that delays an output of the AND gate to output the internal lock signal as a result of the delay.

12. (currently amended) The circuit of claim 1, wherein the FSM stores [[the]] valid detection signals, the valid detection signals including a plurality of first-level and second-level valid detection signals, and

wherein the FSM activates the internal lock signal if [[the]] a number of the first-level valid detection signals is greater than [[the]] a number of the second-level valid detection signals, or else deactivates the internal lock signal.

13. (currently amended) The circuit of claim 1, wherein the data selector selects the first data signal for output if [[the]] an input first or second data signal is a 15_VSB signal, and

wherein the data selector selects one of the first and second data signals based on an operation mode selection signal, if the input first or second data signal is an 8_VSB signal.

14. (currently amended) The circuit of claim 1, wherein the data selector selects the first data signal for output, and then selects the second data signal, in response to the internal lock signal, if an automatic operation mode is selected based on [[the]] an operation mode selection signal, and

wherein the data selector selects one of the first and second data signals for output in response to a data selection signal, if a manual operation mode is selected based on the operation mode selection signal.

15. (currently amended) The circuit of claim 1, wherein the first data signal is received by the data selector from a demodulator, and

wherein the second data signal is received by the data selector from a phase tracking loop.

16. (currently amended) A vestigial side band (VSB) synchronization (sync) signal detection circuit, comprising:

a data selector selecting one of a first data signal and a second data signal for output;

a pseudo-random number 511 (PN511) sequence detection unit receiving the selected first or second data signal, generating a plurality of correlation values for symbols of the received first or second data signal, outputting only those correlation values that exceed a first threshold as correlation values corresponding to a detected ~~Pseudo-random Number (PN)~~ PN511 sequence of a VSB signal, and outputting a first control signal related to sync signal generation;

a buffer unit storing [[the]] a maximum correlation value among the correlation values ~~received from~~ generated by the PN511 sequence detection unit, and generating a second control signal containing information regarding [[the]] a position of a symbol in which the maximum correlation value is generated;

a sync signal position determination unit receiving the second control signal, determining positions of [[a]] next field sync and segment sync signals, and generating a position signal containing information regarding the positions of the next field sync and segment sync signals based on the second control signal;

a pseudo-random number 63 (PN63) correlator receiving the selected first or second data signal from the data selector, detecting correlation values that correspond to a PN63 sequence of the first or second data signal output from the data selector, and generating a sign signal for determining [[the]] a sign of [[the]] a field sync signal; and

a sync signal generator outputting one or more distinct types of sync signals in response to the first control signal, the position signal, and the sign signal.

17. (currently amended) The circuit of claim 16, wherein the data selector selects the first data signal or the second data signal based on one or more of a VSB level selection signal, an operation mode selection signal, a data selection signal, and an external lock signal.

18. (currently amended) The circuit of claim 16, wherein the PN511 sequence detection unit includes:

a sliding PN511 correlator that receives the symbols [[for]] of the selected first or second data signal and generates the correlation values for detecting the PN511 sequence; and

a correlation filter that receives the first threshold, selects correlation values larger than the first threshold for output as the correlation values corresponding to the PN511 sequence, and generates the first control signal for driving the sync signal generator to generate the ~~plurality of~~ one or more distinct types of sync signals[[,]];

wherein the first threshold is provided for detection of [[a]] the field sync signal.

19. (currently amended) The circuit of claim 16, wherein the sync signal position determination unit comprises:

a counting unit that counts [[the]] a number of the symbols so as to determine the positions of the next field sync and segment sync signals, based on the symbol position information for the maximum correlation value contained in the second control signal; and

a calculator generating [[the]] a fourth control signal at a first level, if positions of the next field sync and segment sync signals are determined based on output from the counting unit, or else generating the fourth control signal at a second level.

20. (currently amended) The circuit of claim 19 [[18]], wherein the counting unit further includes:

a first counter that counts 832 symbols to determine the position of the next segment sync signal in response to the second control signal; and

a second counter that counts 313 segments to determine the position of the next field sync signal in response to the second control signal.

21. (currently amended) The circuit of claim 16, wherein the data selector selects the first data signal for output if [[the]] an input first or second data signal is a 15 VSB signal, and

wherein the data selector selects one of the first and second data signals based on an operation mode selection signal, if the input first or second data signal is an 8_VSB signal.

22. (currently amended) The circuit of claim 16, wherein the data selector selects the first data signal for output, and then selects the second data signal, in response to [[the]] an external lock signal, if an automatic operation mode is selected based on [[the]] an operation mode selection signal, and

wherein the data selector selects one of the first and second data signals for output in response to a data selection signal, if a manual operation mode is selected based on the operation mode selection signal.

23. (currently amended) The circuit of claim 16, wherein the first data signal is received by the data selector from a demodulator, and

wherein the second data signal is received by the data selector from a phase tracking loop.

24. (currently amended) A vestigial side band (VSB) synchronization (sync) signal detection circuit, comprising:

means for generating a first control signal related to sync signal generation based on receipt of a selected one of an input first data signal and input second data signal;

means for generating a position signal containing information regarding positions of [[a]] next field sync and segment sync signals;

a correlator for generating a sign signal to determine a sign of [[the]] a field sync signal; and

a generator for generating a plurality of distinct types of sync signals based on the first control signal, position signal, and sign signal.

25. (currently amended) The circuit of claim 24, wherein the means for generating a first control signal includes:

a sliding pseudo-random number 511 (PN511) correlator that receives symbols for the selected first or second data signal and generates correlation values for detecting a PN511 sequence; and

a correlation filter that selects correlation values larger than a [[given]] first threshold for output as correlation values corresponding to the PN511 sequence, and generates the first control signal for driving the generator to generate the plurality of distinct types of sync signals[[,]];

wherein the first threshold is provided for detection of [[a]] the field sync signal.

26. (currently amended) The circuit of claim 25 [[24]], wherein the means for generating a position signal includes:

a buffer unit storing a maximum correlation value among the correlation values ~~received from~~ output by the correlation filter, and generating a second control signal containing information regarding the position of a symbol in which the maximum correlation value is generated; and

a sync signal position determination unit receiving the second control signal, determining positions of [[a]] next field sync and segment sync signals, and generating the position signal based on the second control signal.

27. (currently amended) The circuit of claim 24, wherein the first data signal is selected if the input first or second data signal is a 15_VSB signal, and

wherein one of the first and second data signals is selected based on an operation mode selection signal, if the input first or second data signal is an 8_VSB signal.

28. (currently amended) The circuit of claim 24, wherein the first data signal or the second data signal is selected based on one or more of a VSB level selection signal, an operation mode selection signal, a data selection signal, and an external lock signal.

29. (currently amended) The circuit of claim 28, wherein the first data signal is selected prior to the second data signal, in response to the external lock signal, if an automatic operation mode is selected based on the operation mode selection signal, and

wherein one of the first and second data signals is selected in response to the data selection signal, if a manual operation mode is selected based on the operation mode selection signal.

30. (currently amended) A method of generating one or more vestigial side band (VSB) synchronization (sync) signals, comprising:

selecting one of an input first data signal and an input second data signal for processing;

generating a first control signal for driving sync signal generation based on receipt of the selected first or second data signal;

determining a position signal containing information regarding positions of [[a]] next field sync and segment sync signals;

generating a sign signal to determine a sign of [[the]] a field sync signal; and

outputting a plurality of distinct types of sync signals based on the first control signal, position signal, and sign signal.

31. (currently amended) The method of claim 30, wherein ~~the step of~~ selecting one of an input first data signal and an input second data signal for processing includes:

selecting the first data signal for output, if the input first or second data signal is a 15_VSB signal[[,]]; and

selecting one of the first and second data signals ~~is selected~~ based on an operation mode selection signal, if the input first or second data signal is an 8_VSB signal.

32. (currently amended) The method of claim 30, wherein ~~the step of~~ selecting one of an input first data signal and an input second data signal for processing includes:

selecting the first data signal or the second data signal for output based on one or more of a VSB level selection signal, an operation mode selection signal, a data selection signal, and an external lock signal.

33. (currently amended) The method of claim 32, wherein the first data signal is selected prior to the second data signal, in response to the external lock signal, if an automatic operation mode is selected based on the operation mode selection signal, and

wherein one of the first and second data signals is selected in response to the data selection signal, if a manual operation mode is selected based on the operation mode selection signal.

34. (currently amended) A vestigial side band (VSB) synchronization (sync) signal detection circuit generating a VSB sync signal in accordance with the method of claim 30, wherein the VSB sync signal detection circuit comprises:

an input data signal selector;

a first control signal generator;

a position signal determining device;

a sign signal generator; and

a sync signal output device.